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# Efficiency Evaluation on a CoolMos Switching and IGBT Conducting Multilevel Inverter

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***Abstract*—This paper deals with a three-level inverter topology in the 3 kW range as an alternative to commonly used three-level topologies. The topology is attractive for having low switching losses due to the utilization of CoolMos switching devices while keeping conduction losses low due to the utilization of IGBTs. A proper time delay between the CoolMos and IGBT devices increases the efficiency by 0.2 %. Maximum efficiencies of 97.7 % are achieved and less than 0.2 % efficiency degradation is possible with doubled switching frequency. The case temperatures of the switching devices are below 60 °C at full power.**

***Index Terms*—CoolMOS, IGBT, multilevel inverter, NPC, T-Type**

## I. Introduction

Power electronic converters are important in any electrical power conversion process and high efficiencies are a crucial aspect in the design procedure. In the low voltage applications such as residential grid-tie inverters and frequency converters for drives, a dc-ac inverter is necessary to obtain an ac power that complies with the load specifications. Several topologies are suitable for that and comparisons have shown that three-level inverters show lower total losses compared to their two-level counterparts especially at increased switching frequencies [1], [2]. Among the three-level topologies, the Neutral-Point-Clamped (NPC) and the T-Type (Conergy [3], BSNPC [4]) inverter are commonly used with their own advantages and disadvantages. The NPC can be equipped with semiconductor devices having breakdown voltages of half the DC link voltage only. Therefore switching losses are less affected by the switching frequency. However, an uneven thermal stress occurs among the devices [5], [6]. Due to its low conduction losses, the T-Type inverter shows higher efficiencies at low switching frequencies due to its rather acceptable switching losses. The strong switching frequency dependence, however, is a major drawback of the T-Type inverter due to the implementation of 1200 V Si IGBT switching devices as they have to withstand the whole DC link voltage. One way to reduce the switching losses is to implement next generation's fast switching devices such as Silicon Carbide (SiC) MOSFETs [7], [8] which have superior switching characteristics compared to their Silicon counterparts [9]. Another way towards increasing efficiencies is to combine the NPC and T-Type inverters. Adding two additional CoolMos switches in the T-Type inverter will be used to take over the switching transitions and the conventional 1200 V IGBTs are used afterwards to take over the conduction losses. The topology is referred to as the Hybrid-NPC converter [10], [11] and it is a recently introduced topology without a detailed analysis under which conditions one can benefit from it. The motivation for this work is therefore to investigate such topology in detail and to evaluate its performance in terms of efficiency with respect to chosen switching times between the CoolMos and the IGBT. The paper starts with a description of the inverter topology in Section II including its modulation and the necessary time delay considerations. After that, a loss breakdown analysis is introduced in Section III evaluating performance of the 600 V and 1200 V devices for various switching frequencies. In Section IV, a 3 kW prototype is shown and efficiency curves recorded. Possible efficiency improvements are also shown depending on the chosen time delay. A conclusion is given in Section V.

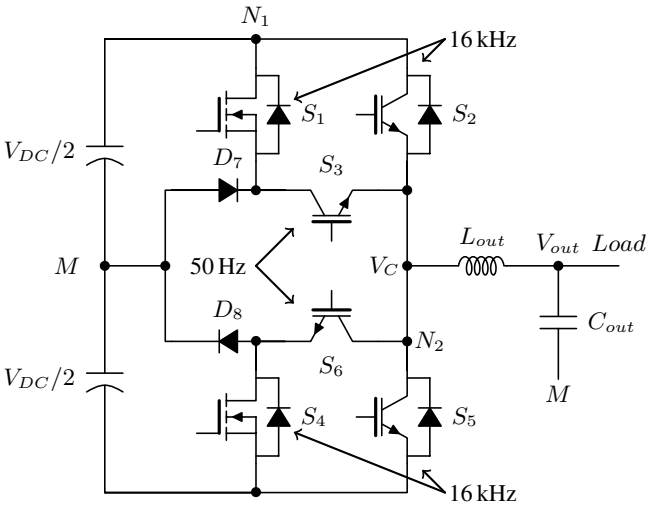



Fig. 1: Single phase schematic of the Hybrid-NPC topology

## II. The hybrid-NPC topology

The Hybrid-NPC topology is a three-level inverter and comprises of six switching devices and two clamping diodes as shown in Fig. 1. The converter output voltage $V_C$ can be

TABLE I: Semiconductors used

| Semiconductors | Device | Voltage in [V] | Current at 25 °C in [A] |
|---|---|---|---|
| $D_8$ and $D_7$ | C3D10060A | 600 V | 29.5 A |
| $S_1$ and $S_4$ | SPP20N60S5 | 600 V | 20 A |
| $S_2$ and $S_5$ | IKW15N120T2 | 1200 V | 30 A |
| $S_3$ and $S_6$ | IKP15N60T | 600 V | 30 A |

either $+V_{DC}/2$, 0 or $-V_{DC}/2$ with $M$ as the reference point. The modulation of this topology is taken from [7] which is the same as for the NPC or T-Type. Only difference is that a necessary time delay $t_d$ between switches $S_1$ and $S_2$ as well as $S_4$ and $S_5$ are added. The idea behind this topology is that switches $S_1$ and $S_4$ are chosen to be 600 V CoolMos devices in order to reduce switching losses. Once the switching transition is over, the voltage across $S_2$ and $S_5$ is reduced to the sum of the voltage drops of $S_1$ and $S_3$ as well as $S_4$ and $S_6$ as shown in (1) and (2).

$$V_{S_2} = V_{S_1} + V_{S_3} \tag{1}$$

$$V_{S_5} = V_{S_6} + V_{S_4} \tag{2}$$

Switches $S_2$ and $S_5$ then turn on with a very small voltage drop resulting in low switching losses. In that way, the large conduction losses of the 600 V CoolMos devices can be reduced by a current divider in the two nodes $N_1$ and $N_2$. The turn on principle for $S_1$ and $S_2$ is shown in Fig. 2. The turn on and turn off logics for $S_1$, $S_2$, $S_4$ and $S_5$ using sine pulse width modulation (SPWM) are shown in Fig. 3.

## III. Simulation Results

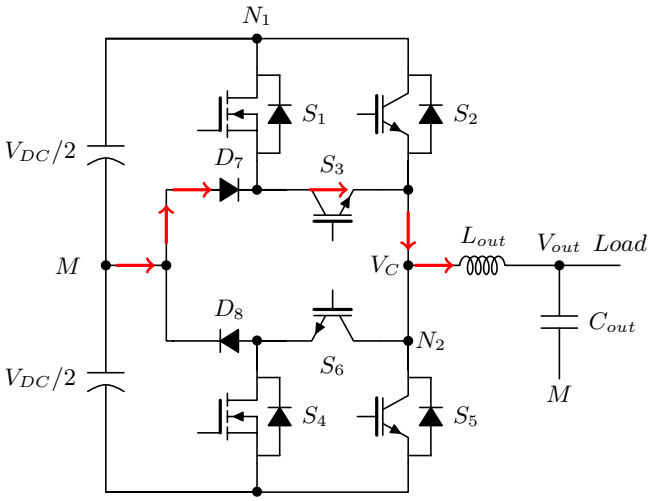
PLECS simulations are conducted in order to evaluate the inverter's efficiency based on the above considerations. A loss breakdown analysis is performed considering the semiconductors used in Table I and the specifications listed in Table II. The results are shown in Fig. 4. It can be seen in Fig. 4b that the switching losses in the converter are mainly occurring in the CoolMos devices because $S_2$ and $S_5$ have a very low voltage during the switching transition and $S_3$ and $S_6$ are operating at grid frequency; i.e. 50 Hz. Hence, the loss increase at increased switching frequencies depends on the switching losses in the CoolMos devices as well as the core and copper losses in the output filter inductor, though the latter is not part of this work since the focus is given to the topology itself.

## IV. Experimental Results

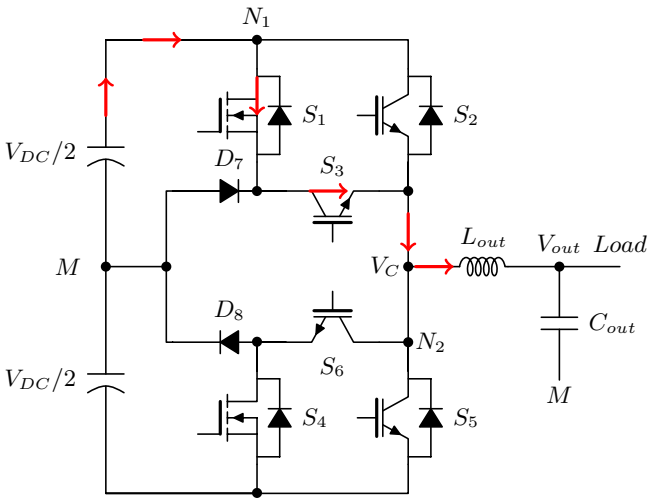
A 3 kW prototype has been built as shown in Fig. 5a. For the sake of simplicity, the gate drivers have been built

TABLE II: Specifications

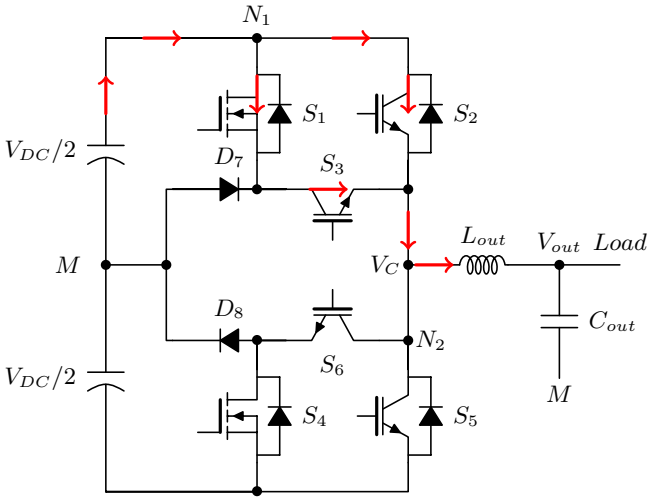
| Symbol | Meaning | Value |
|---|---|---|
| $V_{DC}$ | DC link voltage | 800 V |
| $V_{out}$ | Filtered output voltage, rms | 230 V |
| $P_{out}$ | Output power | 250 W to 3000 W |
| $f_{out}$ | Fundamental frequency | 50 Hz |
| $L_{out}$ | Filter inductor | 3 mH |
| $C_{out}$ | Filter capacitor | 4.4 µF |




(a) Zero output voltage. $S_1$ turned off, $S_2$ turned off




(b) Positive output voltage. $S_1$ turned on, $S_2$ turned off




(c) Positive output voltage. $S_1$ turned on, $S_2$ turned on

Fig. 2: Converter output voltage change from 0 to $+V_{DC}/2$

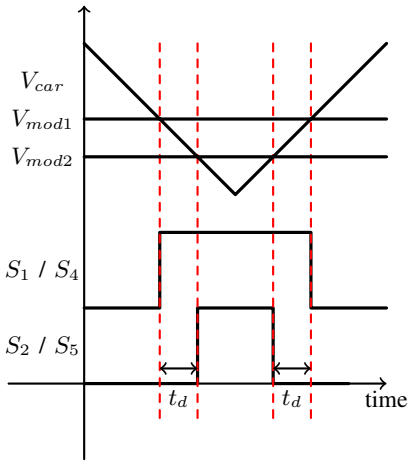
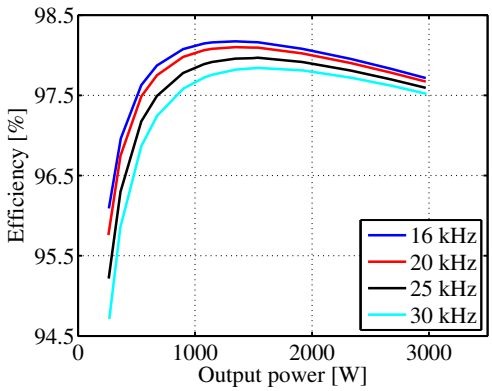
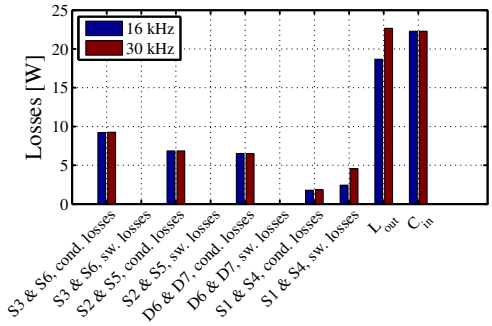



Fig. 3: SPWM implementation with necessary time delays $t_d$




(a) Simulated efficiencies



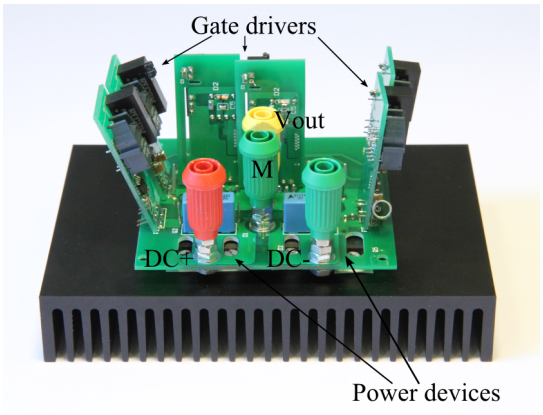

(b) Loss breakdown analysis

Fig. 4: Simulation results of hybrid inverter

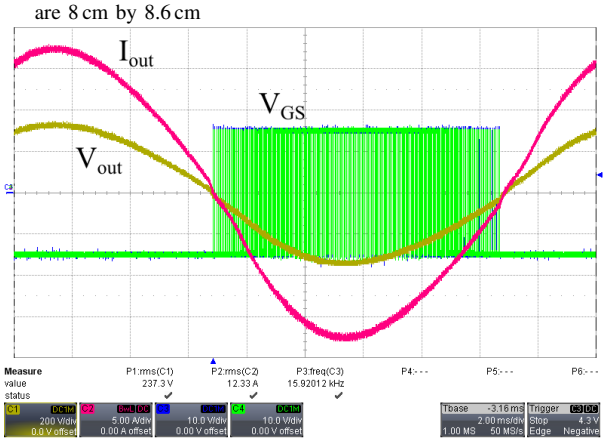
on a separate printed circuit board (PCB) and are mounted vertically to be easily interchangeable. All devices are discrete components, either TO-220 for the 600 V or TO-247 for the 1200 V devices. The filtered output current and voltage as well as the gate signals for $S_4$ and $S_5$ are shown in Fig. 5b.

### A. *Importance of the chosen time delays*

Turn on and turn off switching transitions are captured to see the current commutation between the CoolMos and the



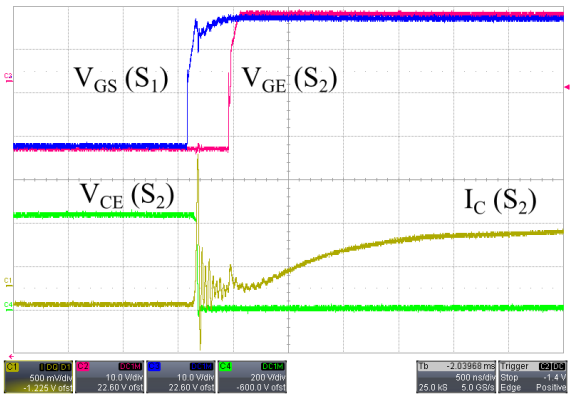

(a) Prototype of the Hybrid-NPC inverter. PCB measurements are 8 cm by 8.6 cm



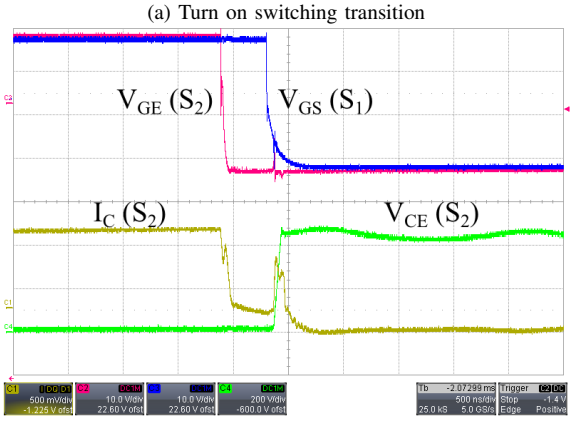

(b) Filtered output waveforms and gate signals at 3 kW and $f_{sw}$ = 16 kHz

Fig. 5: Prototype of Hybrid-NPC inverter in (a) and measured output waveforms and gate signals in (b)

IGBT switching devices. The measurements were started with a time delay of 420 ns and are shown in Fig. 6. The collector current is measured with a Rogowski coil having a bandwidth of 20 MHz and a gain of 100 mV/A. The collector-emitter voltage is measured with a 400 MHz voltage probe and the gate voltages are measured with 500 MHz voltage probes. Figure 6a shows that the voltage across the 1200 V IGBT drops down to a minimum as soon as the CoolMos device is turned on. 420 ns later, the gate command of the IGBT gets high such that the current starts rising. However, it can be seen that the current rise time is rather slow which means that conduction losses still occur in the CoolMos device. By looking at Fig. 6b, it can be seen that the current commutation from the IGBT to the CoolMos device is rather slow, too. However, as soon as the CoolMos device switches, the current commutation progresses much quicker. The reason for that can be explained as follows. When the CoolMos device turns on, the current commutation occurs at a high voltage (in this prototype, the CoolMos device switches the current with 400 V). The voltage drops down to a minimum according to Eq. (2). When the IGBT turns on, the current commutates with a low voltage of a few volts only. Since the IGBT is a bipolar device with a

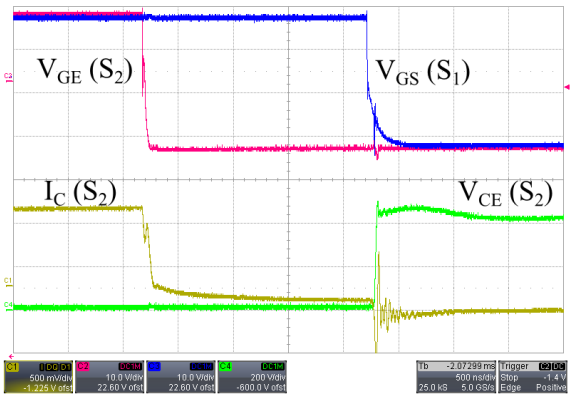



(a) Turn on switching transition

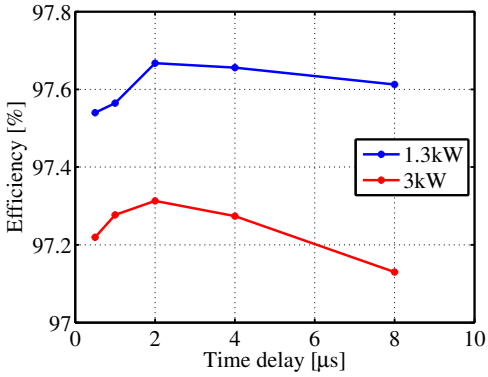



(b) Turn off switching transition

Fig. 6: Turn on and turn off switching transitions with a time delay of 420 ns




(a) Turn off switching transition for a time delay of 2 µs




(b) Efficiencies for different time delays

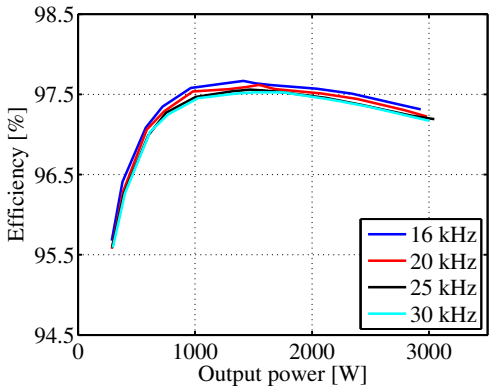
Fig. 7: Turn off switching transition for a larger time delay in (a) and efficiencies for different time delays in (b).

collector current that among others depends on the forward voltage drop of the IGBT (bipolar output characteristic), a rather high dynamic on-resistance might exist. Furthermore, the IGBT is a slower switching device compared to unipolar switches like MOSFETs. Another thing that contributes to the rather slow switching transition of the IGBT are parasitic inductances in the switching loop, both the inductances from the TO-220 and TO-247 packages as well as the inductances due to the PCB layout. In the turn off transition, The IGBT first turns off and the current commutates from the IGBT to the CoolMos device. In addition to the same arguments as before, the tail current contributes to a slow turn off transition. After the specified time delay, the CoolMos device also turns off before the IGBT has fully commutated the current. The consequence is that switching losses also occur in the 1200 V IGBT device. For comparison, the time delay is increased to 2 µs and the turn off transition is repeated, shown in Fig. 7a. Also, efficiencies are measured for different time delays using a N4L PPA5500 power analyzer with a basic accuracy of 0.01 %. For an output power of 1.3 kW and 3 kW and time delays $t_d = 0.42\,\mu s$ to 8 µs, the results are shown in Fig. 7b. It can be concluded that the efficiency clearly depends on the time delay for different output power levels. Choosing the time delay too small, large switching losses will occur in the 1200 V IGBT device. If the time delay is too large, increased conduction losses will occur in the CoolMos device. Highest efficiencies are achieved with a time delay of 2 µs.

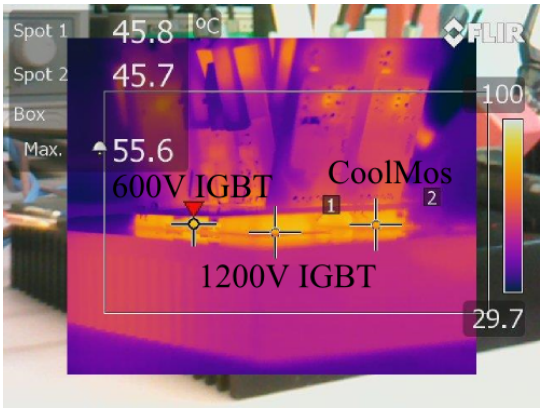
### B. *Efficiency measurements*

Based on the previous analysis, the time delay is set to 2 µs and the efficiency curves for the whole power range and different switching frequencies are shown in Fig. 8a. Maximum efficiency is 97.7 % at 16 kHz and an efficiency degradation of 0.2 % occurs when the switching frequency is increased to 30 kHz. The measured results deviate from the simulated ones. The reason is that the simulations were done under ideal circumstances, i.e. all switches are switching instantly, parasitic inductances in the PCB are neglected. In order to evaluate the stresses on the semiconductor devices, case temperatures of $S_1$, $S_2$ and $S_3$ are measured using an infrared camera. For a switching frequency of 16 kHz, the results can be found in Fig. 8b. The CoolMos and 1200 V IGBT remain relatively cool with a temperature of 45.7 °C and 45.8 °C, respectively. The 600 V IGBT has the highest temperature with 55.6 °C. Increasing the switching frequency up to 30 kHz leads to only a small increase in the case temperatures of the devices as shown in Fig. 8c. Operating at 3 kW and 30 kHz, maximum case temperature is increased up to 58.3 °C. One can conclude that the Hybrid-NPC topology offers an even temperature distribution between the

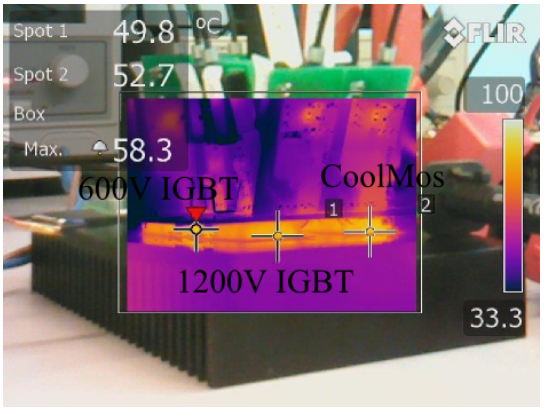
semiconductor devices which is one of the drawbacks of the standard NPC topology. Also, the efficiency is less affected by the switching frequency. Thus, the main drawback of the regular T-Type inverter topology is overcome. However, one must keep in mind that the hybrid mode is only valid for duty cycles greater than the total time delay per switching period.




(a) Measured efficicieny curves for switching frequencies up to 30 kHz and a time delay of 2 µs




(b) Measured temperatures of $S_1$, $S_2$ and $S_3$ at 3 kW and 16 kHz




(c) Measured temperatures of $S_1$, $S_2$ and $S_3$ at 3 kW and 30 kHz

Fig. 8: Measurements of efficiencies in (a) and temperatures for 16 kHz in (b) and temperatures for 30 kHz in (c)

In cases of duty cycles smaller than the specified time delay, the Hybrid-NPC inverter will operate in pure NPC mode, i.e. $S_2$ and $S_5$ will never be turned on.

## V. Conclusion

In this paper, a hybrid topology is investigated to be an alternative for commonly used three-level inverters. The advantage of such topology is to keep the switching losses in the 600 V CoolMos devices while limiting the conduction losses mostly to the 1200 V IGBT devices. An even loss distribution between the semiconductors is therefore possible. However, the drawback of the topology is to be more complex as two more switching devices are needed and critical time delays between the CoolMos and IGBT devices are necessary in order to fully benefit from the complexity. Choosing too small time delays will result in additional switching losses also in the IGBTs; choosing the time delay too large, conduction losses in the CoolMos devices will increase and hence overall efficiency will be decreased again. With a time delay of 2 µs, maximum efficiencies of 97.7 % can be achieved in a 3 kW prototype. Maximum case temperature is 55.6 °C on the 600 V IGBT at 16 kHz and 58.3 °C at 30 kHz.

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